WHAT IS CLAIMED IS:

1. A method for tracing instructions in a microprocessor core that supports execution of instructions in a plurality of instruction pipelines, comprising:

holding trace data for one or more instructions in a group of instructions that were issued together until all instructions in said group of instructions should complete; and

transmitting trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions.

2. The method of claim 1, wherein in an instruction pipeline having a fetch stage, a decode stage, an execute stage, a memory stage, an align stage, and a writeback stage, an instruction should complete after said memory stage.

3. The method of claim 1, wherein said transmitting comprises transmitting information that enables a determination of a static schedule position of a first instruction in said group of instructions.

4. The method of claim 3, wherein said transmitting comprises transmitting a program order signal for each of said plurality of instruction pipelines.

5. The method of claim 4, wherein said program order signal includes a multi-bit signal.

6. The method of claim 5, wherein said multi-bit signal identifies a static schedule position for an instruction in a group of instructions.

7. The method of claim 1, wherein said trace data includes program counter information.

8. The method of claim 1, wherein said trace data also includes one or more of load address, load data, store address, and store data information.

9. In a system having a microprocessor core that supports execution of instructions in a plurality of instruction pipelines, a tracing apparatus, comprising:

a buffer configured to store trace data for one or more instructions in a group of instructions that were issued together, said buffer holding said trace data until all instructions in said group of instructions should complete; and

a trace generation module that transmits trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions.

10. The tracing apparatus of claim 9, wherein in an instruction pipeline having a fetch stage, a decode stage, an execute stage, a memory stage, an align stage, and a writeback stage, an instruction should complete after said memory stage.

11. The tracing apparatus of claim 9, wherein said information enables a determination of a static schedule position of a first instruction in said group of instructions relative to a second instruction in said group of instructions.

12. The tracing apparatus of claim 11, wherein said information includes a program order signal for each of said plurality of instruction pipelines

13. The tracing apparatus of claim 12, wherein said program order signal includes a multi-bit signal.

14. The tracing apparatus of claim 13, wherein said multi-bit signal identifies a static schedule position for an instruction in a group of instructions.

15. The tracing apparatus of claim 9, wherein said trace data includes program counter information.

16. The tracing apparatus of claim 14, wherein said trace data also includes one or more of load address, load data, store address, and store data information.

17. A computer program product comprising:

computer-readable program code for causing a computer to describe a buffer configured to store trace data for one or more instructions in a group of instructions that were

issued together, said buffer holding said trace data until all instructions in said group of instructions should complete; and

computer-readable program code for causing a computer to describe a trace generation module that transmits trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions; and

a computer-usable medium configured to store the computer-readable program codes.

18. A method for enabling a computer to generate tracing logic, comprising:

transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe a buffer configured to store trace data for one or more instructions in a group of instructions that were issued together, said buffer holding said trace data until all instructions in said group of instructions should complete; and

computer-readable program code for causing a computer to describe a trace generation module that transmits trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions.

19. The method of claim 18, wherein computer-readable program code is transmitted to said computer over the Internet.

20. A computer data signal embodied in a transmission medium comprising:

computer-readable program code for causing a computer to describe a buffer configured to store trace data for one or more instructions in a group of instructions that were issued together, said buffer holding said trace data until all instructions in said group of instructions should complete; and

computer-readable program code for causing a computer to describe a trace generation module that transmits trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions.

21. A method for tracing instructions in a microprocessor core that supports execution of instructions in a plurality of instruction pipelines, comprising:

generating trace data that is associated with a plurality of instructions having a program order, each of said plurality of instructions being executed by one of a plurality of instruction pipelines, wherein said generated trace data includes program order information that enables a trace capture component to determine a relative order between instructions that were completed out of order by respective instruction pipelines.